REMARKS

Claims 1-21, 24, and 26-30 stand rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 6,128,747 ("Thoulon") in view of U.S. Patent No. 5,692,204 ("Rawson"). Claims 22, 23, 25, 31, and 32 stand rejected under 35 U.S.C. §103 as being unpatentable over Thoulon in view of Rawson and U.S. Patent No. 6,055,643 ("Chaiken").

The applicants respectfully submit that the examiner inappropriately combined Thoulon and Rawson. To establish a prima facie case of obviousness under 35 U.S.C. §103, there must be a reasonable expectation of success. See M.P.E.P. §706.02(j). However, as explained below, Thoulon and Rawson cannot be combined with a reasonable expectation of success.

Thoulon describes an "electronic device comprising a processor responsive to a sleep signal being asserted to emit an acknowledgement signal and enter a low power mode" (col. 2, lines 18-21). The device is directed to "the problem of setting both the processor and the memory into a sleep or a low power mode" (col. 4, lines 30-32).

The examiner argues that the device of Thoulon wakes the memory from the low power mode without the need for the processor itself to specifically issue the commands needed to control the sleep mode of the memory. Thoulon discusses the following approaches to waking up the memory, and in each approach the processor has been set in a sleep mode:

> According to a first approach applicable to arrangements where the sleep signal is a signal applied to dedicated pin(s) of the processor and is held asserted throughout the time the processor is to be kept in its sleep mode, the sleep control means 15 for setting the memory into the low power mode are also arranged to detect and monitor the sleep signal, and are responsive to this sleep signal being deasserted to wake up the memory from its low power mode. Col. 4, lines 40-48 (emphasis added).
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> An extension to this approach is to have the sleep control means 15 delay propagation of the de-assertion of the sleep signal to the processor till the memory 13 is woken up. Col. 4, lines 51-53. This ensures that the memory is woken up and operative when the processor wakes up. Col. 4, lines 57-58 (emphasis added).
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> In a second approach to memory wake-up, the sleep control means 15 for setting the memory to the low power mode are responsive to transactions being exchanged on the bus to wake up the memory from its low power mode. Col. 4, lines 59-62. Another advantage of this approach is that the memory may be

temporarily woken up for memory accesses that do not require wake-up of the processor. Col. 4, line 67, to col. 5, line 3 (emphasis added).

The examiner then attempts to add to Thoulon an incompatible approach described by Rawson. Specifically, the examiner cites the following from Rawson:

> Other prior art solutions use a cooperative approach wherein hardware communicates, via system firmware, with a central power management executive in the operating system to manage the power state of system devices. ... In this approach both system firmware and specifically enabled power management-aware applications communicate with a central power management executive. Power management event notification messages are passed up from devices through the power management extended system firmware to the power management executive and requests for system power state transitions are passed down from the applications software. Col 1, lines 44-60 (emphasis added).

That approach, described by Rawson, is incompatible with the apparatus of Thoulon, because Rawson's approach includes communication between applications software and a central power management executive in the operating system, which could not happen while the processor is in a sleep mode. There can be no reasonable expectation that the approach of Rawson could successfully be combined with the apparatus of Thoulon as suggested by the examiner, because applications software could not communicate with a central power management executive in the operating system while the processor is in a sleep mode.

In the Advisory Action mailed on August 2, 2004, the examiner contends that "Rawson teaches that power management event notification messages are communicated between the power-managed devices and power management extended system firmware" in column 1, lines 44-63, and that "Rawson explains how such a hardware-based power management power controller operates, sensing power events from and sending power state-changing signals to the power-managed devices, particularly while the system is in a sleep mode" in column 3, lines 42-54. The applicants respectfully argue that the examiner's contention is not correct. The first portion of Rawson cited by the examiner describes a prior art approach to power management that uses "a power management executive in the operating system" (col. 1, lines 46-47). In this prior art approach the processor cannot be in a sleep mode, because the operating system software must be running. The second portion of Rawson cited by the examiner describes a power

management controller of the preferred embodiment of Rawson's approach to power management. This second cited portion of Rawson is not, as suggested by the examiner, an explanation of the first cited portion of Rawson, and, to the extent that it might suggest the possibility of an approach to power management that might be used while the processor is in a sleep mode, any such approach is entirely distinct from the prior art approach of the first cited portion of Rawson.

Furthermore, a prior art reference must be considered in its entirety, i.e., as a whole. See M.P.E.P. §2141.02. Although Rawson describes the power management controller as "providing some residual event sensing capability" that "is particularly useful during times when the central processor is not functioning due to having been placed in a low-power state in order to save power" (col. 3, lines 42-46), there is no further discussion anywhere in Rawson of the processor being in a low-power state. On the contrary, the approach of Rawson is directed to use by operating system software when application software is running and the processor is not in a sleep mode. In the words of Rawson, "the power management features of the present invention are utilized by operating system software which provides optimal utilization of electrical power under varying user application workloads" (col. 3, lines 55-58). As a whole, the approach of Rawson is an approach to power management for use when the processor is not in a sleep mode.

Therefore, once again, there cannot be a reasonable expectation that the approach of Rawson could successfully be combined with the apparatus of Thoulon as suggested by the examiner. Rawson's approach, as a whole, is an approach to power management for use when operating system software and application software are running on the processor, and would not be usable while the processor is in a sleep mode, as described by Thoulon.

Therefore, the combination of Thoulon and Rawson is inappropriate and cannot be used to render the applicants' invention obvious, with or without the additional reference of Chaiken. For this reason, the applicants respectfully request the withdrawal of all of the rejections based on the combination of Thoulon and Rawson, and, since there are no rejections that are not based on the combination of Thoulon and Rawson, the applicants respectfully request the allowance of claims 1-10 and 12-32.

CONCLUSION

Based on the foregoing, the applicant respectfully submits that all of the rejections have been overcome and that claims 1-10 and 12-32 are in condition for allowance. The applicant therefore respectfully requests the issuance of a Notice of Allowance. If there is a deficiency in fees, please charge our Deposit Account No. 50-0221.

Respectfully submitted,

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